

In the Claims:

1. (Previously Presented) An integrated circuit including a capacitor, the integrated circuit comprising:
 - an insulating layer overlying a substrate;
 - a semiconductor layer overlying the insulator layer;
 - a bottom electrode formed in a first portion of the semiconductor layer;
 - a channel region formed in a second portion of the semiconductor layer, the channel region being disposed between a source region and a drain region;
 - a capacitor dielectric overlying the bottom electrode, the capacitor dielectric comprising a high permittivity dielectric having a dielectric constant greater than about 5;
 - a gate dielectric overlying the channel region;
 - a top electrode overlying the capacitor dielectric; and
 - a gate electrode overlying the gate dielectric.
2. (Previously Presented) The integrated circuit of claim 1 wherein the capacitor is a decoupling capacitor.
3. (Previously Presented) The integrated circuit of claim 2 wherein the top electrode is connected to a power supply line and the bottom electrode is connected to a ground line.
4. (Previously Presented) The integrated circuit of claim 1 wherein the top electrode is connected to a first power supply line and the bottom electrode is connected to a second power supply line.

5. (Previously Presented) The integrated circuit of claim 1 wherein the bottom electrode or the top electrode is substantially flat.
6. (Previously Presented) The integrated circuit of claim 1 wherein the top electrode comprises poly-crystalline silicon.
7. (Previously Presented) The integrated circuit of claim 1 wherein the top electrode comprises a metal selected from the group consisting of molybdenum, tungsten, titanium, tantalum, platinum, and hafnium.
8. (Previously Presented) The integrated circuit of claim 1 wherein the top electrode comprises a metal nitride selected from the group consisting of molybdenum nitride, tungsten nitride, titanium nitride, tantalum nitride, and combinations thereof.
9. (Previously Presented) The integrated circuit of claim 1 wherein the top electrode comprises a metal silicide selected from the group consisting of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, tantalum silicide, platinum silicide, erbium silicide, and combinations thereof.
10. (Previously Presented) The integrated circuit of claim 1 wherein the top electrode comprises a metal oxide selected from the group consisting of ruthenium oxide, indium tin oxide, and combinations thereof.

11. (Previously Presented) The integrated circuit of claim 1 wherein the high permittivity dielectric comprises hafnium oxide.
12. (Previously Presented) The integrated circuit of claim 1 wherein the high permittivity dielectric comprises a material selected from the group consisting of aluminum oxide, hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, zirconium silicate, and combinations thereof.
13. (Previously Presented) The integrated circuit of claim 1 wherein the high permittivity dielectric has a relative permittivity of greater than about 10.
14. (Previously Presented) The integrated circuit of claim 1 wherein the high permittivity dielectric has a relative permittivity of greater than about 20.
15. (Previously Presented) The integrated circuit of claim 1 wherein the capacitor dielectric has a physical thickness of less than about 100 angstroms.
16. (Previously Presented) The integrated circuit of claim 1 wherein the capacitor dielectric has a physical thickness of less than about 20 angstroms.
17. (Previously Presented) The integrated circuit of claim 1 wherein the capacitor has a width of larger than about 5 microns.

18. (Previously Presented) The integrated circuit of claim 1 wherein the capacitor has a width of larger than about 10 microns.
19. (Previously Presented) The integrated circuit of claim 1 wherein the capacitor has a length of larger than about 1 micron.
20. (Previously Presented) The integrated circuit of claim 1 wherein the capacitor has a length of larger than about 5 microns.
21. (Previously Presented) The integrated circuit of claim 1, further comprising at least one bottom electrode contact region electrically coupled to the bottom electrode, wherein the bottom electrode contact region is doped to a first conductivity type and wherein the bottom electrode is doped to a second conductivity type and wherein a supply voltage is coupled to the integrated circuit so as to create an inversion region of the first conductivity type in the bottom electrode.
22. (Previously Presented) The integrated circuit of claim 1, further comprising at least one bottom electrode contact region electrically coupled to the bottom electrode, wherein the bottom electrode and the bottom electrode contact region are doped to a first conductivity type.
23. (Previously Presented) A decoupling capacitor comprising:
a semiconductor substrate comprising a silicon surface layer;

a substantially flat bottom electrode formed in a portion of the silicon surface layer,
wherein the bottom electrode is doped to a first conductivity type;

a doped region formed within the silicon surface layer adjacent to the bottom electrode,
the doped region doped to a second conductivity type;

a capacitor dielectric overlying the bottom electrode, the capacitor dielectric comprising a
high permittivity dielectric with a relative permittivity greater than about 5; and

a substantially flat top electrode overlying the capacitor dielectric,

wherein the top electrode is electrically coupled to a first reference voltage line and the
bottom electrode is electrically coupled to a second reference voltage line.

24. (Currently Amended) The decoupling capacitor of claim 23 wherein the top electrode is
connected to a power supply line and the bottom electrode is connected to a ground line.

25. (Currently Amended) The decoupling capacitor of claim 23 wherein the top electrode is
connected to a first power supply line and the bottom electrode is connected to a second power
supply line.

26. (Currently Amended) The decoupling capacitor of claim 23 wherein the semiconductor
substrate is a bulk silicon substrate.

27. (Currently Amended) The decoupling capacitor of claim 23 wherein the semiconductor
substrate is a silicon-on-insulator substrate.

28. (Currently Amended) The decoupling capacitor of claim 23 wherein the top electrode comprises silicon.

29. (Currently Amended) The decoupling capacitor of claim 23 wherein the top electrode comprises a metal selected from the group consisting of molybdenum, tungsten, titanium, tantalum, platinum, and hafnium.

30. (Currently Amended) The decoupling capacitor of claim 23 wherein the top electrode comprises a metal nitride selected from the group consisting of molybdenum nitride, tungsten nitride, titanium nitride, tantalum nitride, and combinations thereof.

31. (Currently Amended) The decoupling capacitor of claim 23 wherein the top electrode comprises a metal silicide selected from the group consisting of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, tantalum silicide, platinum silicide, erbium silicide, or combinations thereof.

32. (Currently Amended) The decoupling capacitor of claim 23 wherein the high permittivity dielectric comprises hafnium oxide.

33. (Currently Amended) The decoupling capacitor of claim 23 wherein the high permittivity dielectric comprises a material selected from the group consisting of hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, zirconium silicate, and combinations thereof.

34. (Currently Amended) The decoupling capacitor of claim 23 wherein the high permittivity dielectric has a relative permittivity of greater than 10.

35. (Currently Amended) The decoupling capacitor of claim 23 wherein the high permittivity dielectric has a relative permittivity of greater than 20.

36. (Currently Amended) The decoupling capacitor of claim 23 wherein the capacitor dielectric has a physical thickness of less than about 100 angstroms.

37. (Currently Amended) The decoupling capacitor of claim 23 wherein the capacitor dielectric has a physical thickness of less than about 50 angstroms.

38. (Currently Amended) The decoupling capacitor of claim 23 wherein the capacitor dielectric has a physical thickness of less than about 10 angstroms.

39. (Currently Amended) The decoupling capacitor of claim 23 wherein the capacitor has a width of larger than about 5 microns.

40. (Currently Amended) The decoupling capacitor of claim 23 wherein the capacitor has a width of larger than about 10 microns.

41. (Currently Amended) The decoupling capacitor of claim 23 wherein the capacitor has a length of larger than about 1 micron.

42. (Currently Amended) The decoupling capacitor of claim 23 wherein the capacitor has a length of larger than about 5 microns.

43. Canceled.

44. (Currently Amended) The decoupling capacitor of claim 23 wherein the first conductivity type is n-type and the second conductivity type is p-type.

45. (Currently Amended) The decoupling capacitor of claim 23 wherein the first conductivity type is p-type and the second conductivity type is n-type.

46. Canceled.

47. (Currently Amended) The decoupling capacitor of claim 23 ~~and~~ further comprising spacers formed on sides of the top electrode.

48. (Currently Amended) The decoupling capacitor of claim 47 ~~and~~ further comprising an etch-stop layer overlying the top electrode and the spacers.

49. (Currently Amended) The decoupling capacitor of claim 48 wherein the etch-stop layer comprises silicon nitride.

50. (Currently Amended) The decoupling capacitor of claim 48 ~~and~~ further comprising an inter-layer dielectric overlying the etch-stop layer.

51. (Currently Amended) The decoupling capacitor of claim 50 wherein the inter-layer dielectric comprises silicon oxide.

52. (Currently Amended) The decoupling capacitor of claim 50 wherein the inter-layer dielectric comprises a dielectric with a relative permittivity less than about 3.5.

53. (Currently Amended) The decoupling capacitor of claim 50 wherein the inter-layer dielectric comprises a dielectric with a relative permittivity less than about 3.0.

54. (Currently Amended) The decoupling capacitor of claim 50 wherein the inter-layer dielectric is selected from the group consisting of benzocyclobutene (BCB), SILK, FLARE, methyl silsesquioxane (MSQ), hydrogen silsesquioxane (HSQ), and SiOF.

55. (Currently Amended) The decoupling capacitor of claim 50 ~~and~~ further comprising a first contact plug in electrical contact with the bottom electrode and a second contact plug in electrical contact with the top electrode.

56. (Currently Amended) The decoupling capacitor of claim 23 further comprising a shallow trench isolation region adjacent to the bottom electrode.

57. (Currently Amended) The decoupling capacitor of claim 23 wherein semiconductor substrate comprises a semiconductor-on-insulator (SOI) substrate and wherein the silicon surface layer includes a plurality of islands, wherein the islands are isolated from one another by mesa isolation.

58-93. Canceled.

94. (Previously Presented) The integrated circuit of claim 1 wherein the gate dielectric is formed from the same material as the capacitor dielectric.

95. (Previously Presented) The integrated circuit of claim 94 wherein the high permittivity dielectric comprises hafnium oxide.

96. (Previously Presented) The integrated circuit of claim 94 wherein the high permittivity dielectric comprises a material selected from the group consisting of hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, zirconium silicate, and combinations thereof.

97. (Previously Presented) The integrated circuit of claim 1 wherein the gate electrode is formed from the same layer as the top electrode.

98. (Previously Presented) A decoupling capacitor comprising:
a semiconductor substrate comprising a silicon surface layer;
a substantially flat bottom electrode formed in a portion of the semiconductor surface layer, wherein the bottom electrode is doped to a first conductivity type;
doped regions formed in the silicon surface layer, the doped regions doped with the first conductivity type;
a capacitor dielectric overlying the bottom electrode, the capacitor dielectric comprising a high permittivity dielectric with a relative permittivity greater than about 5;
a substantially flat top electrode overlying the capacitor dielectric; and
wherein the top electrode is electrically coupled to a first reference voltage line and the bottom electrode is electrically coupled to a second reference voltage line.
99. (Currently Amended) The decoupling capacitor of claim 98 wherein the top electrode is connected to a power supply line and the bottom electrode is connected to a ground line.
100. (Currently Amended) The decoupling capacitor of claim 98 wherein the top electrode is connected to a first power supply line and the bottom electrode is connected to a second power supply line.
101. (Currently Amended) The decoupling capacitor of claim 98 wherein the semiconductor substrate is a bulk silicon substrate.

102. (Currently Amended) The decoupling capacitor of claim 98 wherein the semiconductor substrate is a silicon-on-insulator substrate.

103. (Currently Amended) The decoupling capacitor of claim 98 wherein the top electrode comprises silicon.

104. (Currently Amended) The decoupling capacitor of claim 98 wherein the top electrode comprises a metal selected from the group consisting of molybdenum, tungsten, titanium, tantalum, platinum, and hafnium.

105. (Currently Amended) The decoupling capacitor of claim 98 wherein the top electrode comprises a metal nitride selected from the group consisting of molybdenum nitride, tungsten nitride, titanium nitride, tantalum nitride, or combinations thereof.

106. (Currently Amended) The decoupling capacitor of claim 98 wherein the top electrode comprises a metal silicide selected from the group consisting of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, tantalum silicide, platinum silicide, erbium silicide, or combinations thereof.

107. (Currently Amended) The decoupling capacitor of claim 98 wherein the high permittivity dielectric comprises hafnium oxide.

108. (Currently Amended) The decoupling capacitor of claim 98 wherein the high permittivity dielectric comprises a material selected from the group consisting of hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, zirconium silicate, and combinations thereof.

109. (Currently Amended) The decoupling capacitor of claim 98 wherein the high permittivity dielectric has a relative permittivity of greater than 10.

110. (Currently Amended) The decoupling capacitor of claim 98 wherein the high permittivity dielectric has a relative permittivity of greater than 20.

111. (Currently Amended) The decoupling capacitor of claim 98 wherein the capacitor dielectric has a physical thickness of less than about 100 angstroms.

112. (Currently Amended) The decoupling capacitor of claim 98 wherein the capacitor dielectric has a physical thickness of less than about 50 angstroms.

113. (Currently Amended) The decoupling capacitor of claim 98 wherein the capacitor dielectric has a physical thickness of less than about 10 angstroms.

114. (Currently Amended) The decoupling capacitor of claim 98 wherein the capacitor has a width of larger than about 5 microns.

115. (Currently Amended) The decoupling capacitor of claim 98 wherein the capacitor has a width of larger than about 10 microns.

116. (Currently Amended) The decoupling capacitor of claim 98 wherein the capacitor has a length of larger than about 1 micron.

117. (Currently Amended) The decoupling capacitor of claim 98 wherein the capacitor has a length of larger than about 5 microns.

118. (Currently Amended) The decoupling capacitor of claim 98 ~~and~~ further comprising spacers formed on sides of the top electrode.

119. (Currently Amended) The decoupling capacitor of claim 118 ~~and~~ further comprising an etch-stop layer overlying the top electrode and the spacers.

120. (Currently Amended) The decoupling capacitor of claim 119 wherein the etch-stop layer comprises silicon nitride.

121. (Currently Amended) The decoupling capacitor of claim 119 ~~and~~ further comprising an inter-layer dielectric overlying the etch-stop layer.

122. (Currently Amended) The decoupling capacitor of claim 121 wherein the inter-layer dielectric comprises silicon oxide.

123. (Currently Amended) The decoupling capacitor of claim 121 wherein the inter-layer dielectric comprises a dielectric with a relative permittivity less than about 3.5.

124. (Currently Amended) The decoupling capacitor of claim 121 wherein the inter-layer dielectric comprises a dielectric with a relative permittivity less than about 3.0.

125. (Currently Amended) The decoupling capacitor of claim 121 wherein the inter-layer dielectric is selected from the group consisting of benzocyclobutene (BCB), SILK, FLARE, methyl silsesquioxane (MSQ), hydrogen silsesquioxane (HSQ), and SiOF.

126. (Currently Amended) The decoupling capacitor of claim 121 ~~and~~ further comprising a first contact plug in electrical contact with the bottom electrode and a second contact plug in electrical contact with the top electrode.

127. (Currently Amended) The decoupling capacitor of claim 98 further comprising a shallow trench isolation region adjacent to the bottom electrode.

128. (Currently Amended) The decoupling capacitor of claim 98 wherein semiconductor substrate comprises a semiconductor-on-insulator (SOI) substrate and wherein the silicon surface layer includes a plurality of islands, wherein the islands are isolated from one another by mesa isolation.